IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Bheem Patel et al.	Examiner:	Unknown
Serial No.:	Unknown	Group Art Unit:	Unknown
Filed:	Herewith	Docket:	884.936US1
Title:	VARIABLE-DELAY SIGNAL GENERATORS AND METHODS OF OPERATION THEREFOR		
Assignee:	Intel Corporation	Customer No.:	21186

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 19-0743 in order to have this Information Disclosure Statement considered.

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

BHEEM PATEL ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 349-9592

Date Dec. 30, 2003 By Ann M. McCrack.
Ann M. McCrackin
Reg. No. 42,858

"Express Mail" mailing label number: EV 370239538 US
Date of Deposit: December 30, 2003
This paper or fee is being deposited on the date indicated above with the United States Postal Service pursuant to 37 CFR 1.10, and is addressed to The Commissioner for Patents, Mail Stop Patent Application, P.O. Box 1450, Alexandria, VA 22313-1450.

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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known

Application Number	Unknown
Filing Date	Even Date Herewith
First Named Inventor	Patel, Bheem
Group Art Unit	Unknown
Examiner Name	Unknown

Sheet 1 of 1

Attorney Docket No: 884.936US1

US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
	US-5,148,381	09/15/1992	Sprague, David L.	364	723	02/07/1991
	US-5,489,864	02/06/1996	Ashuri, Roni	327	161	02/24/1995
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	US-6,121,808	09/01/2000	Gaudet,	327	231	
	US-6,348,826	02/19/2002	Mooney, Stephen R., et al.	327	270	06/28/2000

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T[2]

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		DONNELLY, K. S., et al., "A 660MB/s Interface Megacell Portable Circuit in -.3 μm-0.7 μm CMOS ASIC", IEEE Journal of Solid-State Circuits, Vol. 32, (Dec. 1996),1995-2003	
		HAYCOCK, MATTHEW , et al., "A 2.5Gb/s Bidirectional Signaling Technology", Hot Interconnects Symposium V, (Aug. 1997),pp. 1-8	
		LEE, THOMAS H., et al., "A 2.5 V CMOS Delay-Locked Loop for an 18 Mbit, 500 Megabyte/s DRAM", IEEE Journal of Solid-State Circuits, Vol. 29, (Dec. 1994),1491-1496	
		SIDIROPOULOS, STEFANOS , et al., "A Semidigital Dual Delay-Locked Loop", IEEE Journal of Solid-State Circuits, Vol. 32, (Nov. 1997),1683-1692	

EXAMINER **DATE CONSIDERED**

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached